ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit comprises therein a plurality of logic circuits synchronously designed to operate in synchronization with a clock signal, a first power supply wire for supplying a high-potential side power supply voltage from a first input terminal to each logic circuit, a second power supply wire for supplying the high-potential side power supply voltage from a second input terminal to each logic circuit and a third power supply wire for supplying the high-potential side power supply voltage from a third input terminal to each logic circuit. The logic circuit (DFF circuit) includes two stages of latch circuits and a clock signal inversion circuit. Only the clock signal inversion circuit is connected with the first power supply wire, while the second power supply wire is connected with the remaining latch circuits.